REMARKS/ARGUMENTS

Reconsideration and re-examination are hereby requested.

The claims have been provisionally rejected for obviousness double patenting. This issued will be addressed when allowable subject matter is found.

The claims stand rejected under 35 USC 103 as being unpatentable over Martin et al. (U. S. Patent No. 5,214,768) in view of Gaskins (U. S. Patent No. 5,903,911).

The Examiner admits that Martin et al. does not describe a cache memory, a message network operative independently of the data transfer section and wherein the first and second directors control data transfer between the first and second directors in response to messages passing between the first and second directors through the message network.

The Examiner points to Gaskins et al, Figures 2, 3 and 4 and column 7, lines 2-34, column 14 lines 4-18 and column 4 lines 39-40 as somehow teaching a message network operative independently of the data transfer section, and points to figure 2 element 208. However, element 208 is a CACHE MEMORY CONTROLLER not a message network operative independently of the data transfer section and wherein the first and second directors control data transfer between the first and second directors in response to messages passing between the first and second directors through the message network

The Examiner seems to be indicating that adding a cache memory to Martin et al, will increase the bandwidth of the Martin et al. system. It is respectfully submitted that by adding a cache memory to the system of Martin et al. will decrease the bandwidth of the Martin et al. system. Applicants recognized that by having an arrangement having a message network for having messages operative independently of the memory will increase the bandwidth of the system. Applicant's recognition is not described or suggested in either Martin et al. or Gaskins taken either singly or in combination

With regard to the bandwidth teaching in Gaskins, the Examiner points to column 4, lines 30-39. However, reading further, Gaskins points out that:

> In an attempt to increase the bandwidth of the system bus, an alternative prefetch technique may be employed. In this alternative technique, if the

> microprocessor initiates a write cycle and a cache miss occurs, the word is written directly into an allocated block of the cache memory (rather than into system memory). The cache controller concurrently initiates a burst read request to prefetch and store the remaining words of the block from system memory into the cache memory. Although this technique decreases the duration of signal activity on the system bus (since a write cycle to system memory is unnecessary), an incoherency arises since the word written to cache memory was not updated in system memory. The corresponding block of cache memory must accordingly be marked as "dirty".

Applicant fails to see how this has anything to do with providing an arrangement where messages by-passing the data transfer section or is operative independently of the memory increases the bandwidth of the system.

The Examiner takes the position that it is ***inherent*** to combine the first directors into a plurality of director boards. It is respectfully submitted that this is not inherent.

Before discussing the claims and how they distinguish over the cited art, perhaps it might be helpful to review features of Applicant's invention.

Referring to FIG. 2 of the patent application, data passes between the host computer and disk drives through the global cache memory 220 with messages passing between the directors through the message network 260. Thus, the messages do not pass through the global cache memory, whereas the data does pass through the global cache memory.

Referring to FIG. 5 of the patent application, the message network 260 includes a pair of cross bar switches 308. There are a plurality of front end directors on printed circuit boards 190 each connected to a cross bar switch 320. There are also a plurality of back end directors on printed circuit boards 190 each connected to a cross bar switch 320. The cross bar switches 320 are connected to the cross bar switches 308 of the message network 160..

More particularly, it is noted that each crossbar switch 320 has a ***pair*** of ports 325_1 ***AND*** 325_2. Further, it is noted that there are TWO crossbar switches 308 in the message network 160.

Claim 1-15 and claim 30 point out that each one of the boards has a ***PAIR*** of "output/input ports" and that the message network is coupled to the ***pair*** of output/input ports

of the director boards. Such is not INHERENT in Martin et al.

Further, such is not obvious over the claims in patent application serial no. 09/540,828.

Applicant respectfully requests that the Examiner point out:

(1) which element in Martin et al. does the Examiner consider the cache memory; and

(2) which element in Martin et al. does the Examiner consider the cache memory; and

(3) where is there a data transfer between first directors and the second directors ***with such data passing through the cache memory in response*** to messages passing between the first directors and the second directors ***through the messaging network.***

REQUEST FOR TELEPHONE INTERVIEW

If, after reviewing this response, the Examiner still maintains a rejection of the claims, applicant's attorney hereby requests a telephone interview with the Examiner in order to discuss any issues prior to issuing any office action. The Applicant's attorney can be reaches at either the number listed below or at 508 4877 4311.

Referring now to the independent claims:

Claim 1-14 also point out that:

such cache memory being coupled to the plurality of first and second directors;

...

a message network, ***operative independently of the data transfer section,*** coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second ***directors through the message network*** to facilitate data transfer between first directors and the second directors with such data passing through the cache ***memory in the data transfer section.***

Applicant respectfully requests that the Examiner point out where in Martin:

(1) there is the cache memory coupled to the plurality of first and second directors;

(2) there is a message network ***operative independently of the data transfer section;*** and

(3) the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second ***directors through the message network*** to facilitate data transfer between first directors and the second directors with such data passing through the cache ***memory in the data transfer section.***

Similar limitations are in claims 15- 28 and Applicant, with regard to such claims, makes the same request of the Examiner.

Claim 29 points out that:" such messages ***by-passing*** the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section" (emphasis added).

Claim 31 points out that the messages passing through the message network have a destination field. The Examiner points to Gaskins at column 7, lines 66-67 presented below:

The local CPU bus 204 is coupled to an input of comparator 302 for providing a physical address signal from CPU 202. A second input of comparator 302 is

coupled to a tag logic circuit 304.

Such does section of Gaskins doe not describe that messages ***passing through the message network*** have a destination field.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Date

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